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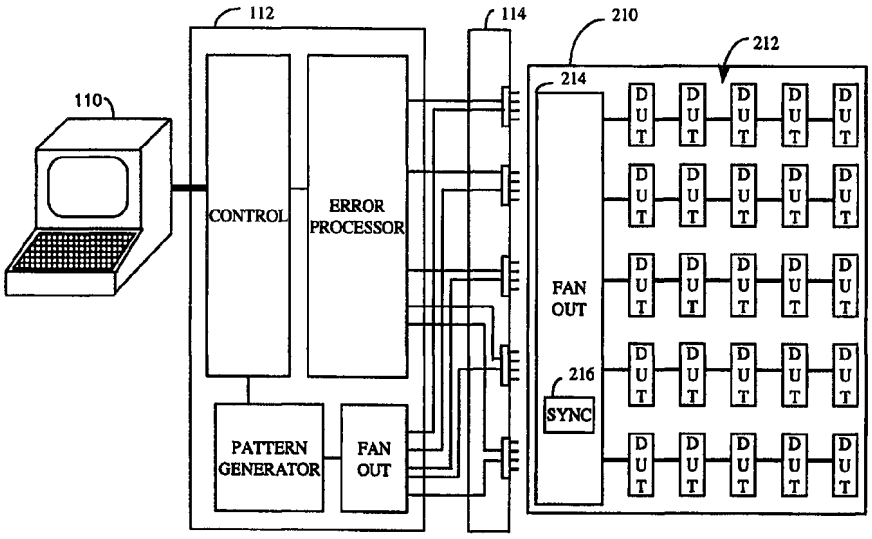

(57) **Abstract**

Automatic test equipment for semiconductor memories that provides testing of large arrays of semiconductor memory chips in parallel. Such massively parallel memory testing greatly enhances test throughput, thereby reducing cost. It greatly enhances the economics of testing memory device made according to a RAMBUS standard, which includes a low speed port and a medium speed port because it allows the same automatic test equipment to economically be used to test devices with the low speed port and the medium speed port.